

1 1. A method for modeling a memory with delay back annotation in accordance with  
2 the VITAL application specific integrated circuit modeling specification, the  
3 method comprising the step of:

4 modeling a path delay of said memory by overloading VITAL path delay  
5 procedures to provide path delay calculations for timing of address,  
6 control, and data bus signals to the memory.

1 2. The method of claim 1 further comprising the steps of:

2 modeling said memory with a timing generic and a port;

3 modeling a wire delay of said memory;

4 modeling a timing check for said memory;

5 modeling functioning of said memory.

1 3. The method of claim 1 wherein modeling of said path delay comprises the step of  
2 overloading VITAL timing check procedures for determining timing constraint  
3 violations of the timing of the address, control, and data bus signals of said  
4 memory.

1 4. The method of claim 1 wherein modeling of said path delay comprises the step of  
2 overloading VITAL wire delay procedures for determining interconnection delay  
3 of the address, control, and data bus signals of said memory.

1 5. The method of claim 1 wherein the memory is selected from a grouping of  
2 memories consisting of SRAM and Flash NVRAM.

1 6. An apparatus for modeling a memory with delay back annotation in accordance  
2 with the VITAL application specific integrated circuit modeling specification, the  
3 apparatus comprising:

4 means for modeling a path delay of said memory by overloading VITAL  
5 path delay procedures to provide path delay calculations for timing of  
6 address, control, and data bus signals to the memory.

1 7. The apparatus of claim 6 further comprising:

2 means for modeling said memory with a timing generic and a port;

3 means for modeling a wire delay of said memory;

4 means for modeling a timing check for said memory;

5 means for modeling functioning of said memory.

1 8. The apparatus of claim 6 wherein the means for modeling of said path delay  
2 comprises means for overloading VITAL timing check procedures for determining  
3 timing constraint violations of the timing of the address, control, and data bus  
4 signals of said memory.

1 9. The apparatus of claim 6 wherein the means for modeling of said path delay  
2 comprises means for overloading VITAL wire delay procedures for determining

3 interconnection delay of the address, control, and data bus signals of said  
4 memory.

1 10. The apparatus of claim 6 wherein the memory is selected from a grouping of  
2 memories consisting of SRAM and Flash NVRAM.

1 11. An electronic design automation system for modeling a memory with delay back  
2 annotation in accordance with the VITAL application specific integrated circuit  
3 modeling specification, the electronic design automation system:

4 a model library storage device which retains a model of a path delay of  
5 said memory, said model of said path delay including an overloading  
6 VITAL path delay procedures to provide path delay calculations for  
7 timing of address, control, and data bus signals to the memory, said  
8 model library storage device connected to an electronic design  
9 automation program execution unit that simulates the path delay of  
10 said memory.

1 12. The electronic design automation system of claim 11 further comprising:

2 a hardware description language storage device connected to the  
3 electronic design automation program execution unit, said hardware  
4 description language storage device retaining:

5 models of said memory with a timing generic and a port;

6 models of a wire delay of said memory;

7 models of a timing check for said memory;

8 models of functioning of said memory; and

1 13. The electronic design automation system of claim 11 wherein the models of said  
2 path delay comprise an overloading of VITAL timing check procedures for  
3 determining timing constraint violations of the timing of the address, control, and  
4 data bus signals of said memory.

1 14. The electronic design automation system of claim 11 wherein the models of said  
2 path delay comprises an overloading of VITAL wire delay procedures for  
3 determining interconnection delay of the address, control, and data bus signals of  
4 said memory.

1 15. The electronic design automation system of claim 11 wherein the memory is  
2 selected from a grouping of memories consisting of SRAM and Flash NVRAM.

1 16. A medium for retaining a computer program which, when executed on a  
2 computing system, executes an electronic design automation process that  
3 describes, evaluates, and simulates a model of a memory with delay back  
4 annotation in accordance with the VITAL application specific integrated circuit  
5 modeling specification, said electronic design automation process comprising the  
6 step of:

7 modeling a path delay of said memory by overloading VITAL path delay  
8 procedures to provide path delay calculations for timing of address,  
9 control, and data bus signals to the memory.

1 17. The medium of claim 16 wherein said electronic design automation process  
2 further comprises the steps of:

3 modeling said memory with a timing generic and a port;

4 modeling a wire delay of said memory;

5 modeling a timing check for said memory;

6 modeling functioning of said memory.

1 18. The medium of claim 16 wherein modeling of said path delay comprises the step  
2 of overloading VITAL timing check procedures for determining timing constraint  
3 violations of the timing of the address, control, and data bus signals of said  
4 memory.

1 19. The medium of claim 16 wherein modeling of said path delay comprises the step  
2 of overloading VITAL wire delay procedures for determining interconnection  
3 delay of the address, control, and data bus signals of said memory.

1 20. The medium of claim 16 wherein the memory is selected from a grouping of  
2 memories consisting of SRAM and Flash NVRAM.